

Method of Checking the Layout versus the Schematic of Multi-fingered MOS Transistor Layouts using a sub-Circuit based Extraction

Abstract of the Invention

A sub-circuit based extraction method which extracts a multi-finger MOS transistor directly as a sub-circuit is described. By adding three marking layers, the method provides the layout extracted netlist with a complete list of device geometric parameters corresponding to the device properties as presented in the sub-circuit model based schematic netlist. By performing a layout-versus-schematic comparison based on all geometric parameters extracted, the layout checking is performed in a complete and accurate way where each device parameter is checked against the corresponding design schematic. This complete and accurate geometric parameter comparison enhances the confidence level of the layout physical verification.